CLAIMS

What is claimed is:

1. A method for sharing hardware resources in a digital system, the method comprising:

determining whether a hardware resource is in use by monitoring contents of at least one of a plurality of semaphore registers; and

accessing said monitored contents of said plurality of semaphore registers by using a limited-width test bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers.

2. The method according to claim 1, further comprising assigning a portion of said limited-width test bus to address each of said plurality of semaphore registers and assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers.

3. The method according to claim 1, where said determination of whether said hardware resource is in use further comprises ORing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 0.

4. The method according to claim 3, further comprising:

if a result of said determination is logic 1, then said hardware resource is in use; and

if a result of said determination is logic 0, then said hardware resource is not in use.

5. The method according to claim 3, further comprising addressing each one of said plurality of semaphore registers by coupling at least one OR gate utilized for said ORing to a bit line in said limited-width test bus.

6. The method according to claim 1, where said determination of whether said hardware resource is in use further comprises ANDing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 1.

7. The method according to claim 6, further comprising:

if a result of said determination is logic 1, then said hardware resource is not in use; and

if a result of said determination is logic 0, then said hardware resource is in use.

8. The method according to claim 6, further comprising addressing each one of said plurality of semaphore registers by coupling at least one AND gate utilized for said ANDing to a bit line in said limited-width test bus.

9. The method according to claim 1, further comprising XORing corresponding register bit locations in each one of said plurality of semaphore registers.

10. The method according to claim 9, further comprising addressing each one of said register bit locations by coupling at least one XOR gate utilized for said XORing to a bit line in said limited-width test bus.

11. The method according to claim 1, further comprising determining from said monitored contents of said plurality of semaphore registers an identifier of a software thread using said hardware resource.

12. The method according to claim 11, further comprising tracking said software thread that is using said hardware resource.

13. A method for sharing hardware resources in a digital system, the method comprising:

arranging a plurality of semaphore registers into a plurality of semaphore register blocks; and

selecting one of said plurality of semaphore register blocks to be accessed by a limited-width test bus.

14. The method according to claim 13, further comprising assigning at least one bit line in said limited-width test bus to select one of said plurality of semaphore register blocks.

15. The method according to claim 14, further comprising:

assigning a portion of remaining bit lines in said limited-width test bus to address each of said plurality of semaphore registers; and

assigning a remaining portion of said limited-width test bus to address each register bit location in said plurality of semaphore registers.

16. The method according to claim 13, further comprising determining whether a hardware resource is in use by ORing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 0.

17. The method according to claim 13, further comprising determining whether a hardware resource is in use by ANDing each register bit location in each of said plurality of semaphore registers if a protocol reset state is logic 1.

18. The method according to claim 13, further comprising determining a software thread identifier by XORing corresponding register bit locations in each one of said plurality of semaphore registers.

19. A system for sharing hardware resources in a digital system, the system comprising:

a plurality of hardware resources;

a plurality of semaphore registers coupled to said plurality of hardware resources; and

a limited-width test bus coupled to said plurality of semaphore registers, wherein said limited-width test bus contains less than a number of bits needed to individually address each of said plurality of semaphore registers.

20. The system according to claim 19, wherein a portion of said limited-width test bus is assigned to address each of said plurality of semaphore registers and a remaining portion to address each register bit location in said plurality of semaphore registers.

21. The system according to claim 19, wherein each register bit in each of said plurality of semaphore registers is coupled to an OR gate.

22. The system according to claim 21, wherein each of said OR gate is coupled to a bit line in said limited-width test bus.

23. The system according to claim 19, wherein each register bit in each of said plurality of semaphore registers is coupled to an AND gate.

24. The system according to claim 23, wherein each of said AND gate is coupled to a bit line in said limited-width test bus.

25. The system according to claim 19, wherein corresponding register bit locations in each one of said plurality of semaphore registers are coupled to an XOR gate.

26. The system according to claim 25, wherein each said XOR gate is coupled to a bit line in said limited-width test bus.

27. The system according to claim 19, wherein a processor coupled to said limited-width test bus determines an identifier of a software thread that is using one of said hardware resources based on contents of at least one of said plurality of semaphore registers.

28. The system according to claim 27, wherein said processor tracks said software thread that is using said hardware resource.

29. A system for sharing hardware resources in a digital system, the system comprising:

a plurality of semaphore register block wherein each of said plurality of semaphore register blocks comprises a plurality of semaphore registers;

a selector coupled to said plurality of semaphore register blocks; and

a limited-width test bus connected to said plurality of semaphore register blocks and said selector.

30. The system according to claim 29, wherein at least one bit line in said limited-width test bus selects one of said plurality of semaphore register blocks.

31. The system according to claim 30, wherein a processor determines whether a hardware resource is in use in said selected one of said plurality of semaphore register blocks.

32. The system according to claim 31, wherein said processor determines an identifier of a software thread using said hardware resource in said selected one of said plurality of semaphore register blocks.

33. The system according to claim 30, wherein said processor tracks said software thread that is using said hardware resource.